CLAIMS

What is claimed is:

1. A method for controlling switching noise in a digital-to-analog interface in a mixed-signal circuit, the digital-to-analog interface including a first plurality (K) of switching elements, said method comprising:

providing a second plurality (M) of dummy switching elements to the digital-to-analog interface, the second plurality (M) being smaller than the first plurality (K);

receiving a digital data signal;

determining a number (N) of the switching elements to be switched for the digital data signal; and

switching the second plurality (M) less the number (N) of the dummy switching elements simultaneously with switching the number (N) of the switching elements.

2. The method of claim 1, further comprising:

estimating a maximum number of the switching elements to be switching simultaneously based on the first plurality (K), a frequency of an operating clock signal of the analog-to-digital interface, and a maximum signal frequency of the mixed-signal circuit; and

setting the second plurality (M) substantially equal to the maximum number.

3. The method of claim 2, wherein the operating clock signal has a frequency greater than the maximum signal frequency of the mixed-signal circuit.

4. The method of claim 1, wherein said determining the first number (N) of the switching elements is based on a difference between a present value and a previous value of the digital data signal.

5. The method of claim 1, wherein the digital-to-analog interface includes a digital-to-analog converter (DAC).

6. A method for controlling switching noise in a digital-to-analog interface in a mixed-signal circuit, the digital-to-analog interface including a first plurality (K) of switching elements and a second plurality (M) of dummy switching elements, the second plurality (M) being smaller than the first plurality (K), said method comprising:

receiving a digital data signal in accordance with an operating clock signal of the analog-to-digital interface;

determining a first number (N) of transitions to be occurred in the first plurality (K) of switching elements based on the digital data signal;

determining a second number by subtracting the first number (N) from the second plurality (M); and

driving the second number of the dummy switching elements simultaneously with switching the first number (N) of the switching elements.

7. The method of claim 6, further comprising:

estimating a maximum number of the switching elements to be switching

simultaneously based on the first plurality (K), a frequency of the operating clock signal, and a maximum signal frequency of the mixed-signal circuit; and

setting the second plurality (M) substantially equal to the maximum number.

8. The method of claim 7, wherein the frequency of the operating clock signal is greater than the maximum signal frequency.

9. The method of claim 6, wherein said determining the first number (N) of transitions comprising;

generating a difference between a present value and a previous value of the digital data signal; and

obtaining an absolute value of the difference.

10. The method of claim 6, wherein said determining the first number (N) of transitions comprising;

performing an exclusive-OR operation on a present value and a previous value of the digital data signal; and

counting non-zero results of the exclusive-OR operation.

11. The method of claim 6, wherein said driving comprising:

toggling the second number of the dummy switching elements.

12. The method of claim 6, wherein the digital-to-analog interface includes a digital-to-analog converter (DAC).

13. A digital-to-analog interface circuit in a mixed-signal circuit, comprising:

an input node adapted to receive an input digital data;

a first plurality (K) of switching elements;

a first encoder coupled to said input node, adapted to generate a first driving signal for the switching elements in accordance with the input digital data;

a second plurality (M) of dummy switching elements;

a delay circuit coupled to said input node, adapted to maintain a previous value of the input digital data;

a differentiator coupled to said input node and said delay circuit, adapted to determine a number (N) of the switching elements to be switched based on a present value and the previous value of the input digital data;

a subtractor coupled to said differentiator, adapted to determine a second number (M-N) by subtracting the number (N) from the second plurality (M) to generate a dummy digital data; and

a second encoder coupled with said subtractor, adapted to generate a second driving signal for the dummy switching elements in accordance with the dummy digital data, the second driving signal switching the second number of the dummy switching elements.

14. The circuit of claim 13, wherein the second plurality (M) is a predetermined maximum number of the switching elements to be switched simultaneously, determined based on the first plurality (K), a frequency of an operating clock signal of the analog-to-digital interface, and a maximum signal frequency of the mixed-signal circuit.

15. The circuit of claim 13, wherein the operating clock signal has a frequency greater than a maximum signal frequency of the mixed-signal circuit.

16. The circuit of claim 13, further comprising:

a limiter circuit coupled to an output of the subtractor, adapted to limit a value of the dummy digital data to zero or greater.

17. The circuit of claim 13, wherein the input digital data includes *k* most significant bits (MSB) for thermometer encoding and remaining bits (LSB) for binary encoding.

18. The circuit of claim 13, wherein each of said switching elements includes a flip-flop, and each of said dummy switching elements includes a toggle flip-flop.

19. The circuit of claim 13, wherein each of said switching elements and said dummy switching elements includes a latch.

20. A digital-to-analog interface circuit in a mixed-signal circuit, comprising:

an input node adapted to receive an input digital data including *k* most significant bits (MSB) for thermometer encoding and remaining *n* bits (LSB) for binary encoding, said input node comprising a first input buffer for the *k* most significant bits and a second input buffer for the remaining *n* bits;

a first plurality (K) of switching elements;

a first encoder coupled to said input node, adapted to generate a first driving signal for the switching elements in accordance with the input digital data, said first encoder including a thermometer encoder for the *k* most significant bits (MSB);

a second plurality (M) of dummy switching elements;

a first differentiator coupled to said first input buffer, adapted to determine a number (N1) of switching elements to be switched based on a present value and the previous value of the *k* most significant bits of the input digital data;

a second differentiator coupled to said second input buffer, adapted to determine a number (N2) of switching elements to be switched based on a present value and the previous value of the remaining *n* bits (LSB) of the input digital data;

an adder adapted to generate a switching number (N) by adding the number (N1) received from the first differentiator and the number (N2) received from the second differentiator;

a subtractor coupled to said adder, adapted to determine a dummy switching number (M-N) by subtracting the switching number (N) from the second plurality (M) to generate a dummy digital data; and

a second encoder coupled with said subtractor, adapted to generate a second driving signal for the dummy switching elements in accordance with the dummy digital

data, the second driving signal switching the second number of the dummy switching elements.

21. The circuit of claim 20, wherein the second plurality (M) is a predetermined maximum number of the switching elements to be switched simultaneously, estimated based on the first plurality (K), a frequency of an operating clock signal of the analog-to-digital interface, and a maximum signal frequency of the mixed-signal circuit.

22. The circuit of claim 20, wherein the operating clock signal has a frequency greater than a maximum signal frequency of the mixed-signal circuit.

23. The circuit of claim 20, further comprising:

a limiter circuit coupled to an output of the subtractor, adapted to limit a value of the dummy digital data to zero or greater.

24. The circuit of claim 20, wherein said first differentiator comprising:

a first delay circuit coupled to said first input buffer, adapted to maintain a previous value of the *k* most significant bits of the input digital data;

a difference generator to generate a difference between the present value and the previous value of the *k* most significant bits of the input digital data; and

an absolute value circuit to generate an absolute value of the difference.

25. The circuit of claim 20, wherein said second differentiator comprising:

a second delay circuit coupled to said second input buffer, adapted to maintain a previous value of the *n* remaining bits of the input digital data;

an exclusive-OR circuit to perform an exclusive-OR operation on the present value and the previous value of the remaining *n* bits of the input digital data; and

a counter to count non-zero bits of an output of the exclusive-OR circuit.

26. The circuit of claim 20, wherein said second encoder comprising:

a thermometer encoder.

27. The circuit of claim 20, wherein each of said switching elements includes a flip-flop, and each of said dummy switching elements includes a toggle flip-flop.

28. The circuit of claim 20, wherein each of said switching elements and said dummy switching elements includes a latch.

29. An apparatus for controlling switching noise in a digital-to-analog interface in a mixed-signal circuit, the digital-to-analog interface including a first plurality (K) of switching elements, said apparatus comprising:

a second plurality (M) of dummy switching elements to the digital-to-analog interface, the second plurality (M) being smaller than the first plurality (K);

means for receiving a digital data signal;

means for determining a number (N) of the switching elements to be switched for the digital data signal; and

means for switching the second plurality (M) less the number (N) of the dummy switching elements simultaneously with switching the number (N) of the switching elements.

30. The apparatus of claim 29, wherein the second plurality (M) is an estimated maximum number of the switching elements to be switched simultaneously, determined based on the first plurality (K), a frequency of an operating clock signal of the analog-to-digital interface, and a maximum signal frequency of the mixed-signal circuit.

31. The apparatus of claim 30, wherein the operating clock signal has a frequency greater than the maximum signal frequency of the mixed-signal circuit.

32. An apparatus for controlling switching noise in a digital-to-analog interface in a mixed-signal circuit, the digital-to-analog interface including a first plurality (K) of switching elements and a second plurality (M) of dummy switching elements, the second plurality (M) being smaller than the first plurality (K), said apparatus comprising:

means for receiving a digital data signal in accordance with an operating clock signal of the analog-to-digital interface;

means for determining a first number (N) of transitions to be occurred in the first plurality of switching elements in an operating clock cycle based on the digital data signal;

means for determining a second number by subtracting the first number (N) from the second plurality (M); and

means for driving the second number of the dummy switching elements simultaneously with switching the first number (N) of the switching elements.

33. The apparatus of claim 32, wherein the second plurality (M) is an estimated maximum number of the switching elements to be switched simultaneously, determined based on the first plurality (K), a frequency of an operating clock signal of the analog-to-digital interface, and a maximum signal frequency of the mixed-signal circuit.

34. The apparatus of claim 33, wherein the frequency of the operating clock signal is greater than the maximum signal frequency.

35. The apparatus of claim 32, wherein said means for determining the first number (N) of transitions comprising:

means for generating a difference between a present value and the previous value of the digital data signal; and

means for calculating an absolute value of the difference.

36. The apparatus of claim 32, wherein said means for determining the first number (N) of transitions comprising:

means for performing an exclusive-OR operation on a present value and the previous value of the digital data signal; and

means for counting non-zero results of the exclusive-OR operation.

37. The apparatus of claim 32, wherein said means for driving comprising:

means for toggling the second number of the dummy switching elements.